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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,068	02/20/2004	Maksim Kuzmenka	2003 P 50080 US	6289

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EXAMINER	
TON, MY TRANG	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,068	KUZMENKA ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8,9 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8,9 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, the limitation "generating a plurality of varyingly strong delayed signals" recited in line 4 is redundant recited with line 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-9 and 15 remain rejected under 35 U.S.C. 102(b) as being anticipated by Morishima (U.S Patent No. 6,046,611) cited in PTOL 1449.

a driver (3) for driving the input signal (input signal applied to 3) comprising a pulse (input pulse) with a positive part and a negative part (high or low) of same duration which encodes the bits (input bits (i.e, 0 or 1) applied to 4).,

a transmission line (1) for transmitting the input signal with an input , which is connected to the driver (3), and an output,

a device (RECEIVER CIRCUIT) for converting the input signal (via 1) into a difference signal, the device (RECEIVER CIRCUIT) comprising a delay member (7) with

an input for receiving the input signal (via 1) and an output (10), for delaying the input signal to obtain a delayed signal and for outputting the delay signal at an output (10), and a differential amplifier (20) with a first input (connected to V1) for receiving the input signal (1), a second input (connected to V10) for receiving the delayed signal (10) and an output for outputting the difference signal formed from the input (1) and the delayed signal (10), and

a termination load, which is connected to the output of the delay member (is inherently seen to read in col. 10, lines 22-24).

Regarding claim 9: the termination load is connected to the output of the delay member via a further transmission line (is inherently seen to read in col. 10, lines 22-24).

The method recited in claim 15 is similarly rejected as claim 8.

Claims 4-6, 8-9, 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Goto (U.S Patent No. 5,589,788).

Goto discloses in Fig. 1 a timing adjustment circuit including:

a delay member (821-827) with an input for receiving the input signal (input applied to 821) and an output (output of 827) for delaying the input signal to obtain a delayed signal and for outputting the delayed signal at an output;

a differential amplifier (9') with a first input (P0) for receiving the input signals, a second input (P7) for receiving the delayed signal and an output for outputting the difference signal formed from the input signal and the delayed signal;

wherein the delay member (821-827) includes a first partial delay member (821-823) with an input (P0) for receiving the input signal and an output for outputting a partially delayed signal (P4) and a second partial delay member (824-827) with an input for receiving the partially delayed signal (connected to P4) and an output (P7) for outputting the delayed signal;

wherein the differential amplifier (9') further comprises an edge detector (940-943) for detecting an edge of the partially delay signal and a comparator (944-947) for determining whether the difference signal is greater than a first predetermined threshold, for determining whether the difference signal is smaller than a second predetermined threshold; and

wherein the differential amplifier is implemented to output a binary signal depending on whether the difference signal is greater than the first predetermined threshold and the partially delayed signal comprises a rising edge or whether the partially delayed signal is smaller than the second predetermined threshold and the partially delayed signal comprises a falling edge (because the structure of the claims is fully met so the functional limitation is also met) as recited in claim 4.

Regarding claim 5: the delay member comprises a plurality of partial delay members (821-827), the differential amplifier (9') comprises a plurality of first inputs for receiving a plurality of first input signals (P0-P3) and a plurality of second input signals for receiving a plurality of second input signals (P4-P7).

Regarding claim 6: the differential amplifier (9') is implemented to select one of the plurality of first input signals (P0-P3) to be the input signal and to select one of the plurality of second input signals (P4-P7) to be the second input signal.

Regarding claims 8-9: a driver (81), a transmission line (line connected to output of 81), a device (82 and 9") comprising a delay member (821-827), and a differential amplifier (9'), a termination load is inherent seen connected to the output of delay (827).

The method recited in claims 13 –14 are similarly rejected as claims 4-6.

The method recited in claim 15 is similarly rejected as claim 8.

Regarding claim 16:

a plurality of partial delay members (821-827), which are connected in series between the input (input connected to 821) and the output of the delay member (output connected to 827), to generate several varyingly strong delayed signals (P0-P7);

a differential amplifier (9') with a first input (P0) for receiving the input signal, a second input (P7) for receiving the delayed signal and an output (FE) for outputting the difference signal formed from the input signal and the delayed signal;

wherein the differential amplifier comprises a plurality of first inputs (output of 940-943) for receiving a plurality of first input signals (P0-P3) and a plurality of second inputs (output of 944-947) for receiving a plurality of second inputs signals (P4-P7) and wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the first input signal and to select one of the plurality of second input signals to be the second input signal (see cols. 6-9); and

wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the input signal and to select one of the plurality of second input signals to be the second input signal depending on the duration of the positive part and of the negative part (high and low) of the bipolar pulse of the input signal (see cols. 6-9) as recited in claim 16.

The method recited in claim 17 is similarly rejected as claim 16: generating a plurality of varyingly strong delayed signals (821-827) and selecting and forming steps in seen to read on element 9'.

Claims 18-20 are similarly rejected as claims 4-6.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-17 are also rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al (U.S Patent No. 6,870,415).

Zhang et al disclose in Fig. 1 a delay generator circuit including:

a plurality of partial delay members (110, 120), which are connected in series between the input (160) and the output of the delay member (120c), to generate several varyingly strong delayed signals (110A-110C, 120A-120C);

a differential amplifier (170) with a first input (110A) for receiving the input signal, a second input (120A) for receiving the delayed signal and an output (172) for outputting the difference signal formed from the input signal and the delayed signal;

wherein the differential amplifier comprises a plurality of first inputs (110A-110B) for receiving a plurality of first input signals and a plurality of second inputs (120A-120C) for receiving a plurality of second inputs signals and wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the first input signal and to select one of the plurality of second input signals to be the second input signal (because the structure of the claims is fully met so the functional limitation is also met); and

wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the input signal and to select one of the plurality of second input signals to be the second input signal depending on the duration of the positive part and of the negative part (high and low) of the bipolar pulse of the input signal (160) (see cols. 2-3) as recited in claim 16.

The method recited in claim 17 is similarly rejected as claim 16: generating a plurality of varyingly strong delayed signals (110-120) and selecting and forming steps in seen to read on element 170.

Response to Arguments

Applicant's arguments filed 11/24/05 have been fully considered but they are not persuasive.

Applicant's argument – a driving circuit of Morishima does not generate a bipolar pulse with a positive part and a negative part of the same duration for providing transmission of a "bit".

Examiner response -- Driving circuit (3) of Morishima clearly shown a bipolar pulse (input pulse) with a positive part and a negative part (high or low) of the same duration (duration at the input and the output of driving circuit 3 is the same) for providing transmission of a "bit" (considered as 0 or 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

February 14, 2006